AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED REVISION TO 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a ~~circuit comprising a~~ plurality of configuration pins ~~inputs~~ configured to receive a plurality of configuration signals generated external to said apparatus;

an input pin; and

a circuit comprising:

a first logic gate configured to generate a first ~~provide a selected device~~ identification signal ~~(ID)~~ from said configuration signals;

a first multiplexer directly connected to said first logic gate to multiplex said first identification signal to a first multiplexer output; and

a shift register comprising a plurality of memory elements ~~different device IDs~~, wherein (i) said shift register is couplable to said input pin and (ii) a first of said memory elements has a first input directly connected to said first multiplexer output such that said first identification signal forms a first portion of a ~~said plurality of inputs allow said circuit to be implemented with any of said plurality of different~~ device identification for said apparatus ~~IDs~~.

2. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~selected device ID comprises a soft code~~ configuration signals are user variable.

3. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein said circuit comprises a JTAG compliant controller.

4. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein each value of said ~~plurality of different~~ device identification ~~IDs~~ identifies a unique configuration of said circuit.

5. (CURRENTLY AMENDED) The apparatus according to claim ~~1~~ 4, wherein said ~~selected~~ device identification determines a storage capacity of said circuit ~~ID can be reconfigured after fabrication of said apparatus~~.

6. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said circuit further comprises:

a second logic gate ~~circuit~~ configured to ~~receive~~ generate a second identification signal from said ~~plurality of inputs~~ configuration signals and;

a second multiplexer directly connected to ~~configured to receive an output of~~ said second logic ~~circuit~~ gate to multiplex said second identification signal to a second multiplexer output, ~~; and~~ wherein a second of said memory ~~element~~ elements has a second input directly connected to ~~configured to receive an output of~~ said second multiplexer output such that said second identification signal forms a second portion of said device identification.

7. (CURRENTLY AMENDED) The apparatus according to claim 6, wherein said second multiplexer is ~~further configured to receive an input signal and a shift signal~~ directly connected to a first memory output of said first memory element.

8. (CURRENTLY AMENDED) The apparatus according to claim 7, wherein said second logic ~~circuit comprises a logic~~ gate performs a NAND operation on said configuration signals.

9. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~apparatus~~ circuit further comprises a FIFO memory.

10. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said ~~plurality of inputs~~ configuration signals comprise mark options.

11. (CANCELLED)

12. (ORIGINAL) The apparatus according to claim 1, wherein said circuit comprises a JTAG device compliant with the IEEE standard 1149.1.

13. (CURRENTLY AMENDED) An apparatus comprising:

means for receiving a plurality of ~~inputs~~ configuration signals generated external to said apparatus; ~~and~~

an input pin;

means for ~~providing a selected device~~ generating a first identification ~~(ID)~~ signal from ~~a plurality of different device IDs~~ said configuration signals;

means for multiplexing said first identification signal from said means for generating to a first output; and

means for storing a plurality of bits (i) couplable to said input pin, wherein (ii) a first of said means for storing has a first input directly connected to said first output such that said first identification signal forms a portion of a ~~said plurality of inputs allow implementation of any of said plurality of different~~ device identification for said apparatus ~~IDs~~.

14. (CURRENTLY AMENDED) A method for selecting ~~one of~~ a device identification for an apparatus, ~~plurality of different device identifications (IDs)~~ comprising the steps of:

(A) receiving a plurality of ~~inputs~~ configuration signals generated external to said apparatus ~~configured to select said one of said~~ at a plurality of ~~different device IDs~~ configuration pins; ~~and~~

(B) generating a first identification signal by performing a logic operation on said configuration signals;

(C) multiplexing said first identification signal to a first memory element of a plurality of memory elements in a shift register couplable to an input pin; and

(D) storing said first identification signal in said first memory element such that said first identification signal forms a first portion of said ~~configuring a device with said selected device identification (ID), wherein said plurality of inputs allow implementation of any of said plurality of different~~ device identification ~~IDs~~.

15. (CURRENTLY AMENDED) The method according to claim 14, wherein said ~~selected device ID comprises a soft code~~ configuration signals are user variable.

16. (CURRENTLY AMENDED) The method according to claim 14, wherein each value of said ~~different~~ device identification ~~IDs~~ identifies a unique ~~circuit~~ configuration of said apparatus.

17. (CURRENTLY AMENDED) The method according to claim 14, wherein said ~~selected~~ device identification ~~ID can be reconfigured after fabrication~~ determines a storage capacity of said apparatus.

18. (CURRENTLY AMENDED) The method according to claim 14, wherein said ~~plurality of inputs~~ configuration signals comprise mark options.

19. (CANCELLED)

20. (CURRENTLY AMENDED) The method according to claim 14, ~~further comprising providing~~ wherein said apparatus is a JTAG device compliant with the IEEE standard 1149.1.

21. (NEW) The apparatus according to claim 1, further comprising an output multiplexer configured to multiplex said device identification from said shift register to an output pin.

22. (NEW) The method according to claim 14, further comprising the step of:

multiplexing said device identification from said shift register to an output pin.